

# Constraint-Based Test Generation

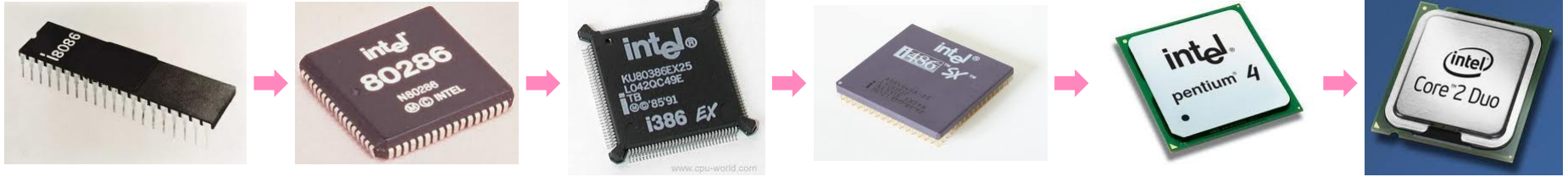
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# A Word About Cadence

- Cadence
  - One of the three major EDA (Electronics Design Automation) companies
  - Established in 1988, over 4000 employees
  - Wide variety of technologies and products in
    - Hardware design (inc. logic synthesis, power, timing, routing, etc.)
    - Hardware simulation
    - Formal and simulation-based verification
  - Never heard about us? You surely heard about our customers.
    - Intel, Cisco, TI, Canon, Phillips, Samsung, Nokia, ...

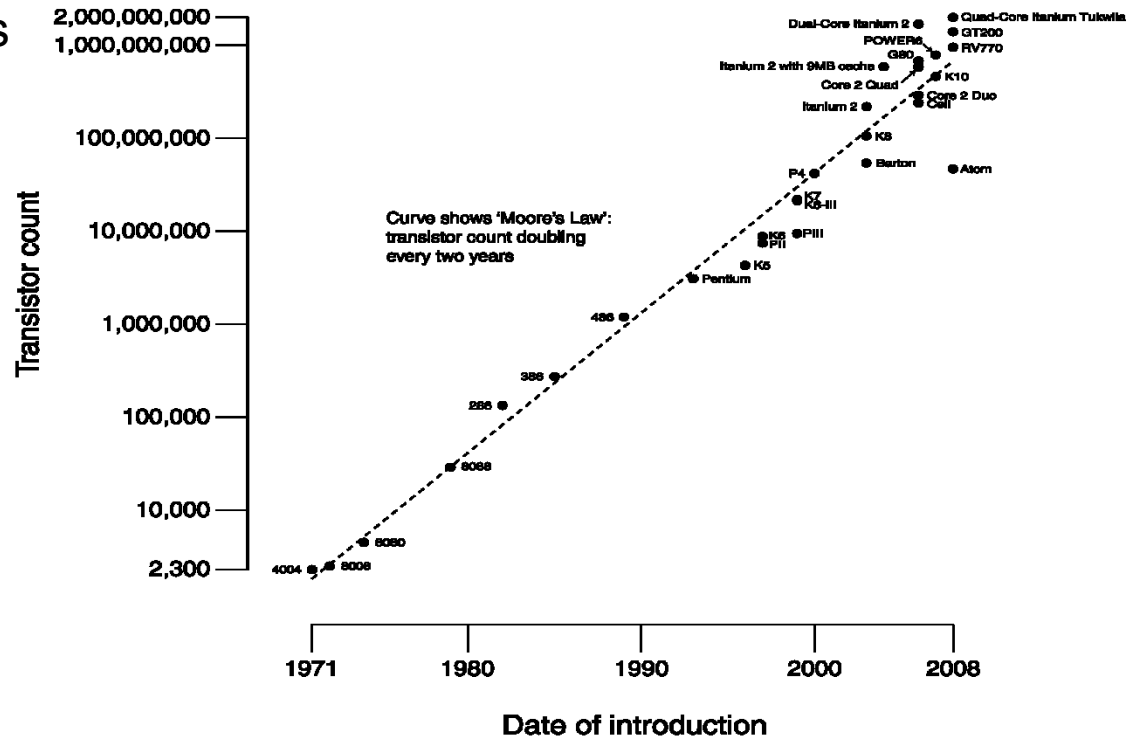
# Motivation



CPU Transistor Counts 1971-2008 & Moore's Law

Chip complexity grows, and so does

- the likelihood of HW bugs
- the cost of HW bugs
- the need for verification
- investment in verification

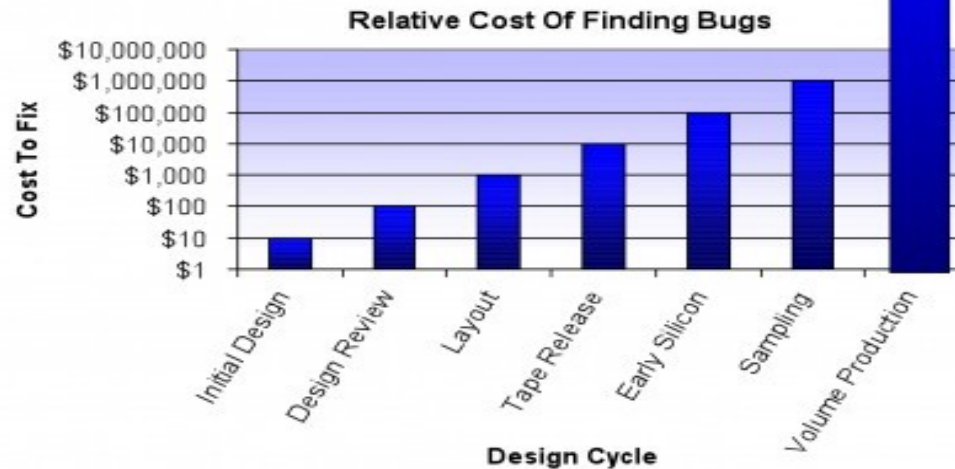


# The Cost of HW Bugs

- Intel FDIV, 1994, ~\$475M
- Intel Sandy Bridge, 2011, ~\$1B

$$\frac{4195835}{3145727} = 1.333820449136241002$$

$$\frac{4195835}{3145727} = 1.333739068902037589$$

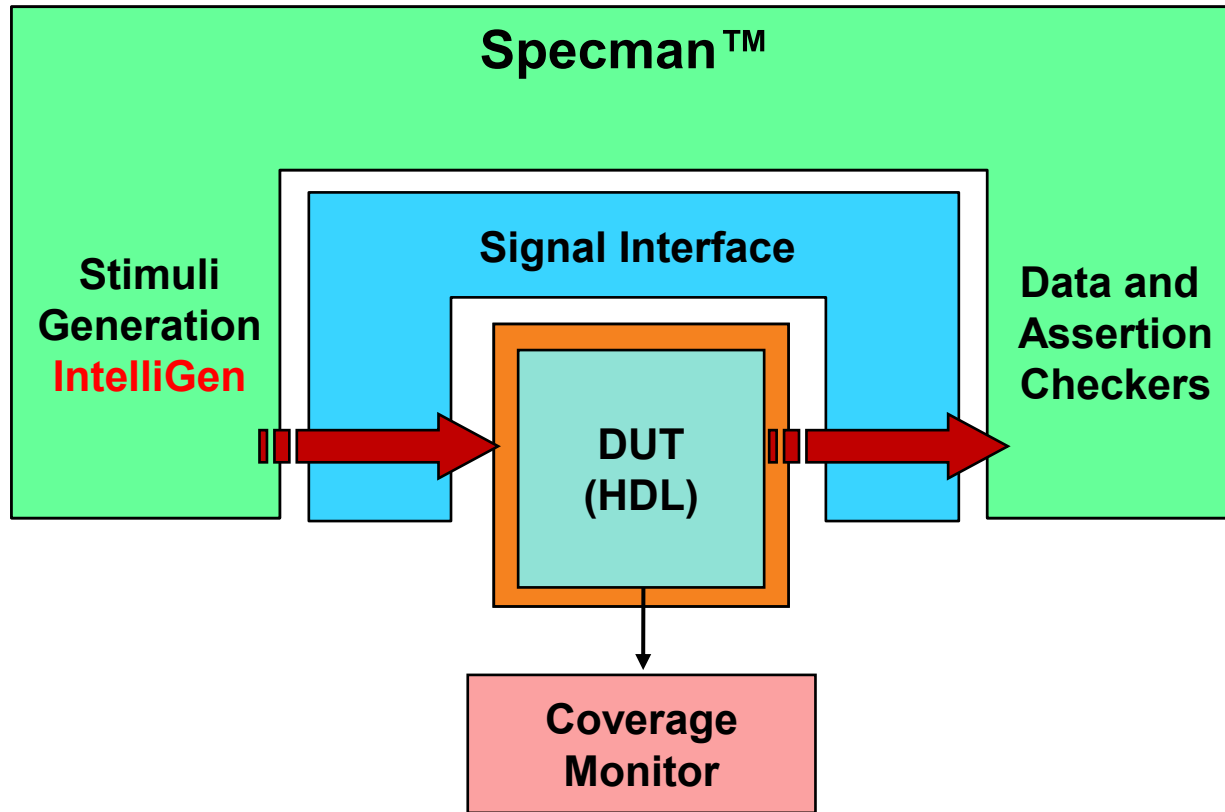


Silicon Debug, Doug Josephson and Bob Gottlieb, (Paul Ryan)  
D. Gizopoulos (ed.), *Advances in Electronic Testing: Challenges and Methodologies*, Springer, 2006

# Formal vs. Simulation

- Formal verification
  - + *Proves* properties of a HW design
  - + Substantial improvements in performance, capacity and scalability in the last few years
    - ✓ Improvements in SAT solvers
    - ✓ New approaches using abstraction and Solving Modulo Theories (SMT)
  - ✗ Cannot verify (yet?) a full system, only individual units
  - ✗ Verification environment cannot be reused for post-silicone testing
- Simulation-based verification
  - + High capacity and scalability
  - + Verification environment can be reused for post-silicone testing
  - + Easy to use
  - ✗ Experimentally verifies properties of a HW design
- **~80%** of bugs in HW logics are still found through simulation

# Verification by Simulation



Package	# Classes	Line Coverage	Branch Coverage	Complexity
All Packages	201	33%	20%	2.26
pkg00001	2	N/A	N/A	1
pkg00002	2	83%	71%	2.017
pkg00003	1	85%	83%	2.233
pkg00004	1	90%	83%	3.051
pkg00005	4	87%	85%	2.122
pkg00006	2	55%	24%	1.488
pkg00007	3	77%	73%	4.905
pkg00008	20	24%	24%	2.129
pkg00009	21	15%	12%	2.181
pkg00010	42	44%	23%	4.024
pkg00011	6	18%	14%	3
pkg00012	10	35%	47%	4.312
pkg00013	6	0%	0%	2.642
pkg00014	19	27%	21%	5.313
pkg00015	19	34%	31%	2.594
pkg00016	1	0%	0%	8.962
pkg00017	23	45%	38%	3.433
pkg00018	32	14%	1%	3.516
pkg00019	21	14%	14%	3.979
pkg00020	1	74%	72%	2.833
pkg00021	3	13%	N/A	4
pkg00022	10	45%	38%	2.887
pkg00023	2	0%	0%	4.871
pkg00024	4	0%	0%	1.668
pkg00025	2	0%	0%	2.4

# Specman

- Cadence's major test bench automation tool
- Being used in the biggest and most advanced verification environments
- Works with all HDL simulators
- Uses **e** verification language [Hollander, Morley, Noy '01]

<http://en.wikipedia.org/wiki/Specman>

# IntelliGen

- Constraint solver / test generator of Specman
  - Generates randomized tests based on constraint models
- Variety of data types:
  - signed/unsigned numeric, Boolean, string, arrays, pointers
- Variety of constraints:
  - arithmetic, logic, bit-wise, soft constraints, global constraints on arrays
- Based on an FD-core
  - Also integrates a few variations of BDD and SAT
- Includes a visual constraint debugger



# Random Test Generation in Specman/e

```
struct CPU_instruction {
  opcode : [LDA, STA, ADD, SUB,
           JMP, JGE, JNE, STP](bits:4);
  operand : uint(bits:12);
  keep opcode == STA => operand > 1023;
};

struct CPU_test {
  program : list of CPU_instruction;
  sz : uint[10..20];
  keep program.size()==sz;
  keep program[sz-1].opcode==STP;
  keep for each (instr) in program {
    index<sz-1 => instr.opcode != STP;
    instr.opcode in [JMP, JGE, JNE] =>
      instr.operand<sz;
  };
};
```

IntelliGen

item	type	opcode	operand
0.	instruction	JMP	6
1.	instruction	JMP	11
2.	instruction	ADD	2301
3.	instruction	JGE	1
4.	instruction	SUB	312
5.	instruction	LDA	2603
6.	instruction	JMP	7
7.	instruction	JGE	11
8.	instruction	JNE	4
9.	instruction	STA	3913
10.	instruction	JMP	12
11.	instruction	SUB	1783
12.	instruction	LDA	2035
13.	instruction	ADD	1310
14.	instruction	JNE	15
15.	instruction	JMP	12
16.	instruction	LDA	3258
17.	instruction	STP	3964

# IntelliGen. The Requirements

- Powerful and flexible constraint language
  - Mixed integer and bitwise models
  - Mixed declarative and procedural code in models (function calls)
  - Non-scalar data: structures, arrays, strings
  - Soft constraints for modeling preferences
  - Directives for controlling randomness and distribution
- High scalability
  - Huge models (hundreds of thousands variables and constraints)
  - Solving the same problem many times (long runs)
- Find many random solutions
  - Try to meet distribution requirements
  - Be *random-stable* as much as possible
- Typical problems are not hard
  - Extensive search is usually not required
  - Backtracks typically indicate bad modeling

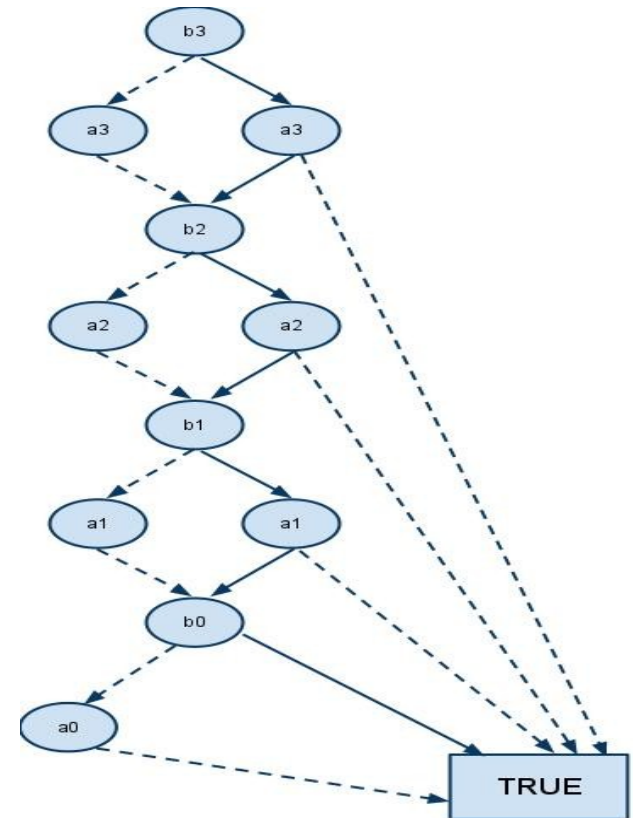
# IntelliGen.

## The Integrated Framework of Solvers

- There is no “best” solving technology.
  - A combined approach is required in practice
- BDD
  - + Bit-level, fast, complete control over the distribution
  - ✗ Capacity problems
- SAT
  - + Fast, scalable
  - ✗ Translation to CNF is expensive, limited control of randomness
- Finite-Domain solver
  - + Word-level, fast, scalable, extendable
  - ✗ Limited control over distribution
  - ✗ Bad in proving UNSAT
- Local Search / SMT / ILP... ?

# Solving Technologies: BDD

- Build the BDD once
- Generate solutions as random walks from the root to TRUE
- + Good performance when generating many solutions
- + Complete control over the distribution
- ✗ Limited capacity
- ✗ Very sensitive to the order of variables
- ✗ Infeasible for some types of constraints



$$\langle a_3, a_2, a_1, a_0 \rangle \leq \langle b_3, b_2, b_1, b_0 \rangle$$

# Solving Technologies: SAT

- Convert the constraint model to a CNF
- Give it to a state-of-the-art SAT solver
- + High capacity
- + High performance
- + Improvements are free
- ✗ Randomization is tricky, no guarantee of distribution
- ✗ High bootstrap cost
- ✗ Loss of high-level context:
  - Role and association of bits
  - No GAC (loss of propagation) e.g., all-different [Bessiere, Katsirelos, Narodytska, Walsh, 09]

$$\begin{aligned} &(\neg a_3 \vee b_3) \wedge \\ &(\neg a_3 \vee r_2) \wedge \\ &(b_3 \vee r_2) \wedge \\ &(\neg r_2 \vee \neg a_2 \vee b_2) \wedge \\ &(\neg r_2 \vee \neg a_2 \vee r_1) \wedge \\ &(\neg r_2 \vee b_2 \vee r_1) \wedge \\ &(\neg r_1 \vee \neg a_1 \vee b_1) \wedge \\ &(\neg r_1 \vee \neg a_1 \vee r_0) \wedge \\ &(\neg r_1 \vee b_1 \vee r_0) \wedge \\ &(\neg r_0 \vee \neg a_0 \vee b_0) \end{aligned}$$

$$\langle a_3, a_2, a_1, a_0 \rangle \leq \langle b_3, b_2, b_1, b_0 \rangle$$

# Solving Technologies: FD Solver

- Maintain *domains* of variables as sets of intervals
  - $x : [1..100]$ ,  $y : [1,3,5..8]$ ;  $z : [1..100,1000..2000]$ ;
- Use propagators to enforce domain consistency
- Combine search and propagation
- *Randomize the choice of variables and values*
  
- + Cheap on simple problems
- + Scales very well to large problems
- + Word-level processing
  - Easy to extend: new constraints, global constraints, randomization policies
  - Easy to explain e.g., in constraint debugger
  
- ✗ Limited control over randomness and distribution
- ✗ Bad in proving UNSAT

# IntelliGen's FD Solver

**Solve**( $V, C$ ) : [TRUE, FALSE]

**if** all variables in  $V$  are assigned **then return** TRUE

choose an unassigned variable  $x$  in  $V$

**repeat**

    choose a value  $k$  from the domain of  $x$

**if** **Propagate**( $V \cdot [x/k]$ ,  $C$ ) && **Solve**( $V$ ,  $C$ ) **then**

**return** TRUE

**else**

        undo the last reduction

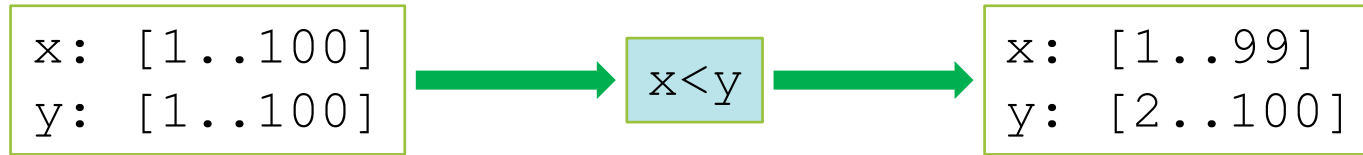
        remove  $k$  from the domain of  $x$

**until** range of  $x$  is empty

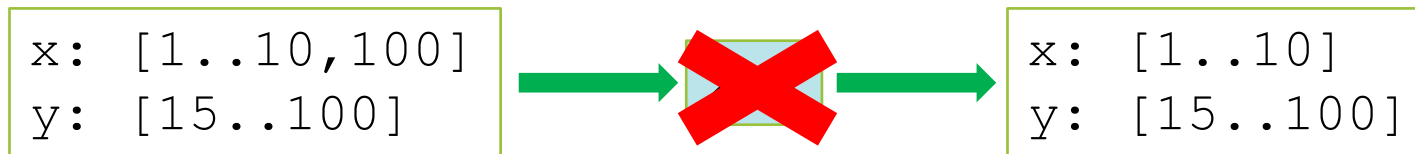
**return** FALSE

# Propagation

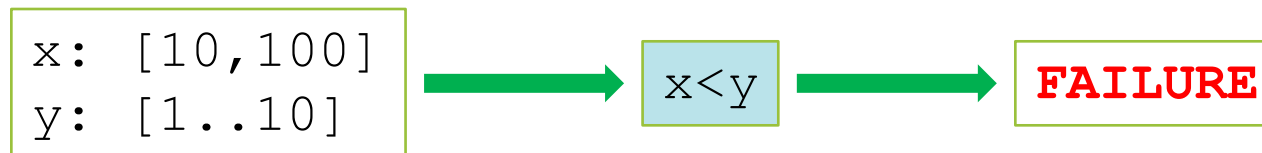
- Removes inapplicable values from domains



- Prunes the model by removing trivially satisfied constraints



- Fails if domains are inconsistent





# More On Propagation

- A more interesting example

$x:[1..100], y:[1..100], x < y \ \&\& \ x * x < 300 \ \&\& \ x + y > 40 \rightarrow x:[1..17], y:[24..100], x + y > 40$

- IntelliGen includes propagation algorithms for

- Relations  $== \ != \ < \ > \ <= \ >=$
- Boolean logic **and or not => ?:**
- Arithmetic  $+ \ - \ * \ / \ \%$
- Bitwise operations  $<< \ >> \ | \ \& \ \sim$
- Arrays (global) constr. `my_list.all_different()`
- Pointers, strings, etc.  $(p==p1 \ \mathbf{or} \ p==p2 \ \mathbf{or} \ p==NULL)$

# The Hybrid Domain Representation

- **Problem:** intervals are inadequate for representing bitwise information
  - The interval representation the domain of x is [0..2, 4..6, 8..10, 12..14...]
  - interval representation has a billion fragments!!!
  - ... and bitmask representation can't help!
- **Solution:**
  - Use a hybrid domain representation combining intervals and BDDs
  - Do lazy updates between the two

```
x: uint;  
keep x[1:0] != 0b11;
```

# BDD Propagation [Lagoon and Stuckey, CP'04]

- Assume a binary constraint  $c(x,y)$  represented by a BDD
- Assume two domains  $d(x)$  and  $d(y)$  of  $x$  and  $y$
- The updated domains  $d'(x)$  and  $d'(y)$  are computed as

$$d'(x) = d(x) \wedge [c(x, y) \wedge d(y)]_x$$

$$d'(y) = d(y) \wedge [c(x, y) \wedge d(x)]_y$$

- The propagation fails if we get FALSE in any conjunction
- The propagator becomes redundant if

$$d(x) \wedge d(y) \Rightarrow c(x, y)$$

- Straightforward extension to any number of variables

# Many Refinements of the Search Mechanism

- Heuristic choice of variable/value
  - Take into account domain size, role, connectivity, etc.
- Smart graph-based backtrack mechanisms
  - Save only the relevant domains before each assignment
  - Save on backtracking through independent sub-graphs
- Restarts
- Local and global backtrack limits
  - Get out of unproductive corners of the hyperspace quickly
  - Stop and signal an error rather than take forever in search

# Gen Debugger

[Alexandron, Lagoon, Naveh and Rich, HVC'09]

- The types of “constraint bugs”
  1. It can't find me a solution
  2. It finds a solution with unexpected values
  3. It never finds a solution with expected values
  4. It takes way too long/forever to find a solution
- The main principles of constraint debugging
  - Visualization
    - See the information you need in a clear and accessible way
  - Navigation
    - Get to the information you need
  - Minimization
    - See only the relevant information

# Visualization

The image shows a screenshot of a design debugger interface with several callout boxes pointing to specific components:

- Menu Bar:** Located at the top, containing options like Edit, View, Navigate, Run, and Options.
- Process Tree:** A tree view on the left showing the hierarchy of the design process, with nodes like CFS: sys.cdn\_uart\_env.uart\_evc.has\_tx'tx\_agent.
- Variables Pane:** A table showing the state of variables in the selected field set. The table has columns for Type, Name, Initial, and Current.
- Constraints Pane:** A pane on the right showing constraints for the selected field set, such as 'keep rx\_agent.p\_sync == value@\_sync@8'.
- Generated Tree:** A tree view at the bottom left showing the generated design structure, including components like sys, vr\_ahb\_instance\_print\_opt, and cdn\_uart\_env.
- Details Pane:** A pane at the bottom right showing the source code for the selected variable, with tabs for General Info, Source, Past Steps, and Constraints.

Type	Name	Initial	Current
<input type="checkbox"/>	Input value(p_sync)		shr_uart_sync-@8
<input type="checkbox"/>	Input has_rx		TRUE
<input type="checkbox"/>	Input has_rx'rx_agent.active_passive		ACTIVE
<input type="checkbox"/>	Input has_rx'rx_agent.direction		RX
<input checked="" type="checkbox"/>	Gen has_rx'rx_agent.ACTIVETX'driver.p_sync		
<input checked="" type="checkbox"/>	Gen has_rx'rx_agent.p_sync		shr_uart_sync-@8

```
Source File: shr_uart_agent.e
13 <'
14
15 unit shr_uart_agent_u {
16   -- Name of the environment
17   env_name: shr_uart_env_name_t;
18
19   agent_name: shr_uart_agent_name_t;
20
21   -- A pointer to the synchronizer
22   p_sync: shr_uart_sync;
23
24   -- A pointer to the env
25   p_env: shr_uart_env_u;
26
27   -- define TX or RX
28   direction: shr_uart_agent_dir_kind_t;
29
30   -- Defines active or passive agent (predefined enum type)
31   active_passive: erm_active_passive_t;
```

# GenDebugger: Navigation

- Re-use the standard concepts of procedural debugging
  - Generation breakpoints / trace-points
    - Stop at any solving step, or at a specific partition, data type, object, field, variable, etc.
  - Step-by-step debugging
    - Step through atomic operations of the FD solver: propagation, assignment, backtrack
    - Walk into or walk over the generation of nested objects
    - Continue to the end of the context or to the next breakpoint
- GUI
  - See the hierarchy of objects, the time line of the generation, the relevant variables, and constraints, the source code
  - Access all constraints of a variable, all variables of a constraint, all past steps for a variable

# GenDebugger: Minimization

- It is essential to minimize explanations:
  - In debugger, explaining propagations
  - In error messages explaining infeasibility
- Conservative minimization
  - Mark only the constraints that caused domain changes or failure
  - + Does not cost anything
  - + Sufficient in most cases
  - ✗ Explanations may have redundancy
- Aggressive minimization
  - Try to remove constraints one by one
  - + Produces a minimal set
  - ✗ Significant performance overhead

```
struct my_data {  
    x : uint;  
    y : uint;  
    z : uint;  
    keep x[4:0] == 0b11111;  
    keep x<y;  
    keep y<z;  
    keep x+y<20;  
    keep x+z<20;  
};
```



# Conclusion

- Verification is important
- Testing/simulation is (still) the main workhorse of verification
- CP is the backbone of today's test generation
- The requirements differ from the "classic" CP
  - Problems are often easy (not much search)
  - Problems are often HUGE (hundreds of thousands elements)
  - Many random solutions required
  - Need to support many data types, including non-scalar
- There is no "best" constraint solving technology
  - Need to combine FD, BDD, SAT, etc. in a unified framework
  - Make different technologies benefit from each other
- Constraint debugging and debuggers are necessary
  - But mostly overlooked by the research community



# Questions





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